WAVESPLITTER™ TECHNOLOGIES, INC.

Data Sheet

400G QSFPDD DR4+ 2km Transceiver Module
P/N: WST-QD4-DR4+C

Features:

- 4x100 Gigabit Ethernet (4x106.25 Gbit/s)
- Compliant to 26.5625 GBd PAM4,
  - 400GAUI-8 (Aggregation mode) and
  - 4x100GAUI-2 (Breakout mode)

  Electrical Interface specifications
- MPO-12 with 8° angled end face
- Low power consumption: 12 W max
- Operating case temperature: 0 to 70 °C
- Two-wire common management interface
- RoHS compliant

Applications:

- Data Center 100GE 2km SMF links
- Switch/Router interconnections

Standards:

- IEEE 100GBASE-FR compliant
- SFF-8636 management interface

Description

Wavesplitter's WST-QD4-DR4+C is a 4x100G QSFP56-DD optical transceiver that enables high 4 parallel 100 GbE port densities owing to its compact size and low power consumption. WST-QD4-DR4+C may be used in network applications, such as Ethernet switches and IP routers, at transmission distances of up to 2 km over parallel single mode fiber (SMF).

The form factor of WST-QD4-DR4+C - QSFP56-DD Type 2 - is compliant with the hardware and management interface specifications (MIS) of the QSFP-DD multi-source agreement (MSA). QSFP-DD modules can support up to eight electrical lanes on the host interface, which is double the number of lanes supported by QSFP28 or QSFP+ modules. The unique feature of QSFP-DD ports is that they are mechanically and electrically compatible with QSFP28 and QSFP+. Hence, the same port can be used to support multiple generations of modules and data rates if the networking hardware is designed for such operation.

WST-QD4-DR4+C transmits data in compliance with the optical interface specification 100GBASE-FR1 defined by IEEE P802.3cu-D2p2 per each lane. 100GBASE-FR1 specifies the use of 4-level pulse amplitude modulation (PAM4) at 53.125 Gbaud operating at each of 4 channels with 1.3 μm wavelength range. The bit rate per lane is 106.25 Gbit/s, which produces a total data rate of 425 Gbit/s in 4 lanes.

The electrical interface is in compliance with 400GAUI-8 specified in IEEE 802.3-2018 Section 8 and 4x100GAUI-2 specified in IEEE 802.3-2018 Section 6/IEEE P802.3cd-2018. 400GAUI-8 specifies the use of eight differential electrical lanes operating at 26.5625 Gbaud PAM4 per lane. The bit rate per lane is 53.125

Gbit/s, resulting in an aggregate data rate of 425 Gbit/s that matches the optical line interface. An internal gear box IC converts between the eight lanes of the host interface and the four lanes of the line interface. 100GAUI-2 specifies the use of two differential electrical lanes operating at 26.5625 Gbaud PAM4 per lane. The bit rate per lane is 53.125 Gbit/s, resulting in a data rate of 106.25 Gbit/s that matches the optical interface per lane. An internal gear box IC converts between the two lanes of the host interface and the one lane of the line interface.

The bit error ratio (BER) of the optical interface is required by 100GBASE-FR1 to be less than 2.4 x 10-4. Hardware using WST-QD4-DR4+C must have RS(544,514) forward error correction (FEC) capability to meet the frame loss ratio requirements. The specification for RS(544,514) FEC may be found in IEEE 802.3-2018 Section 8.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Power Supply Voltage	V_{CC}	0	3.6	V	
Optical Receiver Input (each lane)			+5	dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	°C	
Supply Voltage Noise Tolerance	$PSNR_{mod}$			66	mV	10 Hz –10 MHz
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Power Consumption	P_6			12	W	
Supply Current	Icc-6			1154.4	mA	Steady state
Instantaneous peal current	Icc_ip_6			4800	mA	
Sustained peak current	Icc_sp_6			3960	mA	

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Min	Typical	Max	Units	Notes
Module output (each lane, at TP4) (Note 1)					
Signaling Rate, each Lane	26.5625 ± 100 ppm			GBd	
AC Common-mode output voltage (RMS)			17.5	mV	
Differential peak-to-peak output voltage			900	mV	
Near-end ESMW (Eye symmetry mask width)	0.265			UI	
Near-end Eye height, differential	70			mV	
Far-end ESMW (Eye symmetry mask width)	0.2			UI	
Far-end Eye height, differential	30			mV	
Far-end pre-cursor ISI ratio	-4.5		2.5	%	
Differential output return loss	Equation (83E-2)			dB	2
Common to differential mode conversion return loss	Equation (83E-3)			dB	2
Differential termination mismatch			10	%	
Transition time (20% to 80%)	9.5			ps	
DC common mode voltage	-350		2850	mV	
Module input (each lane)					
Signaling Rate, each Lane	26.5625 ± 100 ppm			GBd	
Differential pk-pk input voltage tolerance	900			mV	at TP1a
Differential input return loss	Equation (83E-5)			dB	at TP1, 2
Differential to common mode input return loss	Equation (83E-6)			dB	at TP1, 2
Differential termination mismatch			10	%	at TP1
ESMW (Eye symmetry mask width)	0.22			UI	at TP1a
Eye width	0.22			UI	at TP1a
Applied pk-pk sinusoidal jitter	Table 120E–6			MHz, UI	at TP1a
Eye height	32			mV	at TP1a
Single-ended input voltage tolerance range	-0.4		3.3	V	at TP1a
DC common mode voltage	-350		2850	mV	at TP1

Notes:

1. Electrical module output is squelched for loss of optical input signal.
2. IEEE Std 802.3-2018 Section 6.

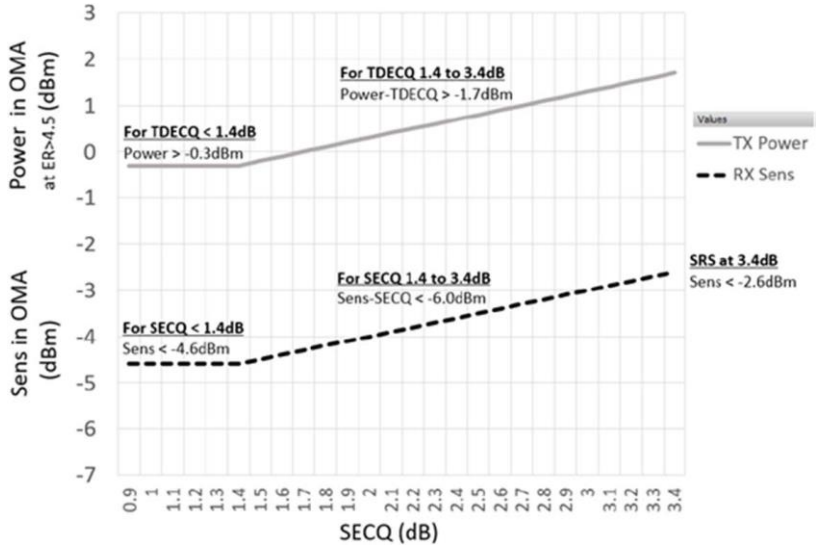
Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						
Wavelength Assignment	λ_C	1304.5		1317.5	nm	
Channel data rate	f_{DC}	106.25			Gbit/s	
Data Rate, each Lane	f_{SG}	53.125 ± 100 ppm			GBd	PSM4
Side-mode suppression ratio	SMSR	30			dB	
Average launch power, each lane		-3.1		4.0	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each lane		0.1		4.2	dBm	for TDECQ <1.4 dB
		-1.5+ TDECQ				for 1.4 dB ≤ TDECQ ≤ 3.4 dB
Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			3.4	dB	
Transmitter eye closure for PAM4, each lane	TECQ			3.4	dB	
| TDECQ – TECQ |				2.5	dB	
Average optical output power of OFF Transmitter, each lane	Poff			-15	dBm	
Extinction Ratio, each lane	ER	3.5			dB	
Transmitter transition time				17	ps	
Transmitter over/under-shoot				22	%	
Transmitter peak-to-peak power				5	dBm	
$RIN_{15.6}OMA$				-136	dB/Hz	
Optical return loss tolerance				17.1	dB	
Transmitter reflectance				-26	dB	2
Receiver						
Average receive power, each lane		–7.1		4	dBm	3
Receive power (OMAouter) ,				4.2	dBm	

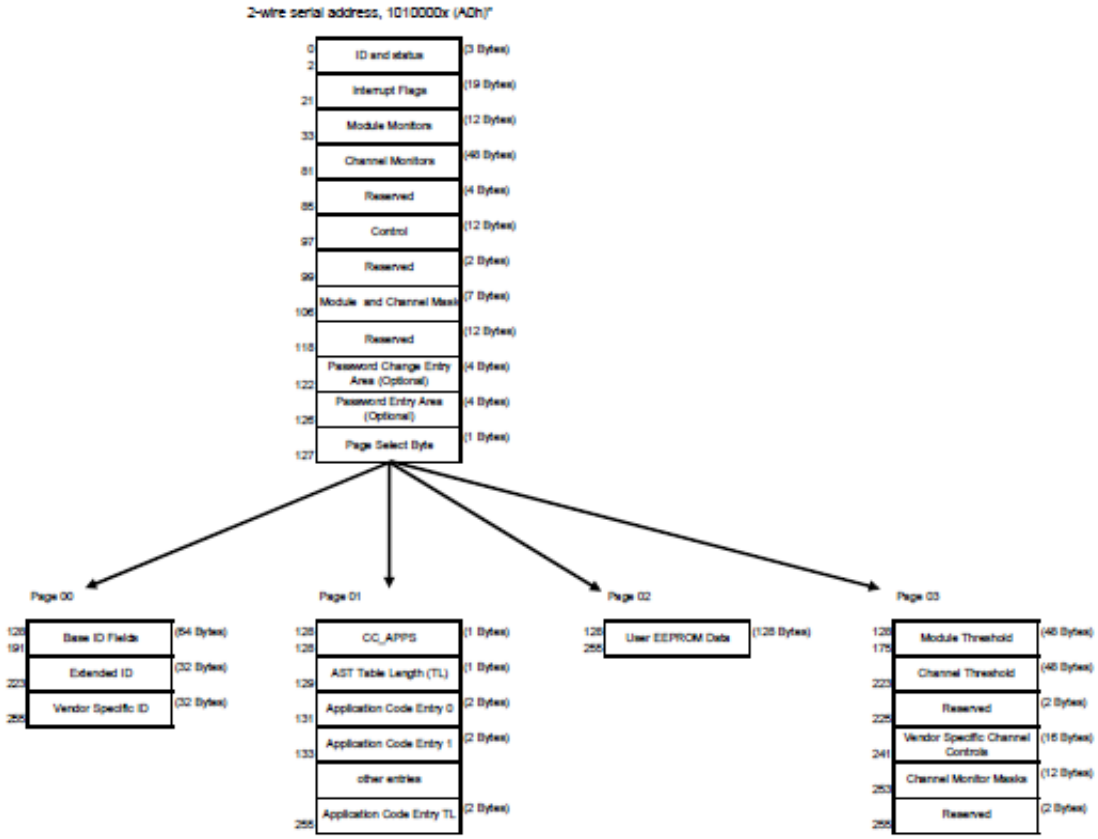
each lane						
Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter), each lane		Max -4.5			dBm	for TECQ <1.4 dB, 4
		Max (-5.9 + TECQ)				for 1.4 dB ≤ TECQ ≤ 3.4 dB, 4
Stressed receiver sensitivity, each lane (OMAouter)				-2.5	dBm	4, 5
Conditions of stressed receiver sensitivity test (note 6)						
Stressed eye closure for PAM4, lane under test	SECQ	3.4			dB	
LOS Assert	LOSA	-15		-8	dBm	
LOS De-assert	LOSD			-7.5	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter reflectance is defined looking into the transmitter.
3. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
4. For when Pre-FEC BER is 2.4 x 10^{-4}.
5. Measured with conformance test signal at TP3 (see IEEE P802.3cu clause 140.7.10) for the BER specified in IEEE P802.3cu clause 140.1.1.
6. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



MEMORY MAP



Digital Diagnostic Functions

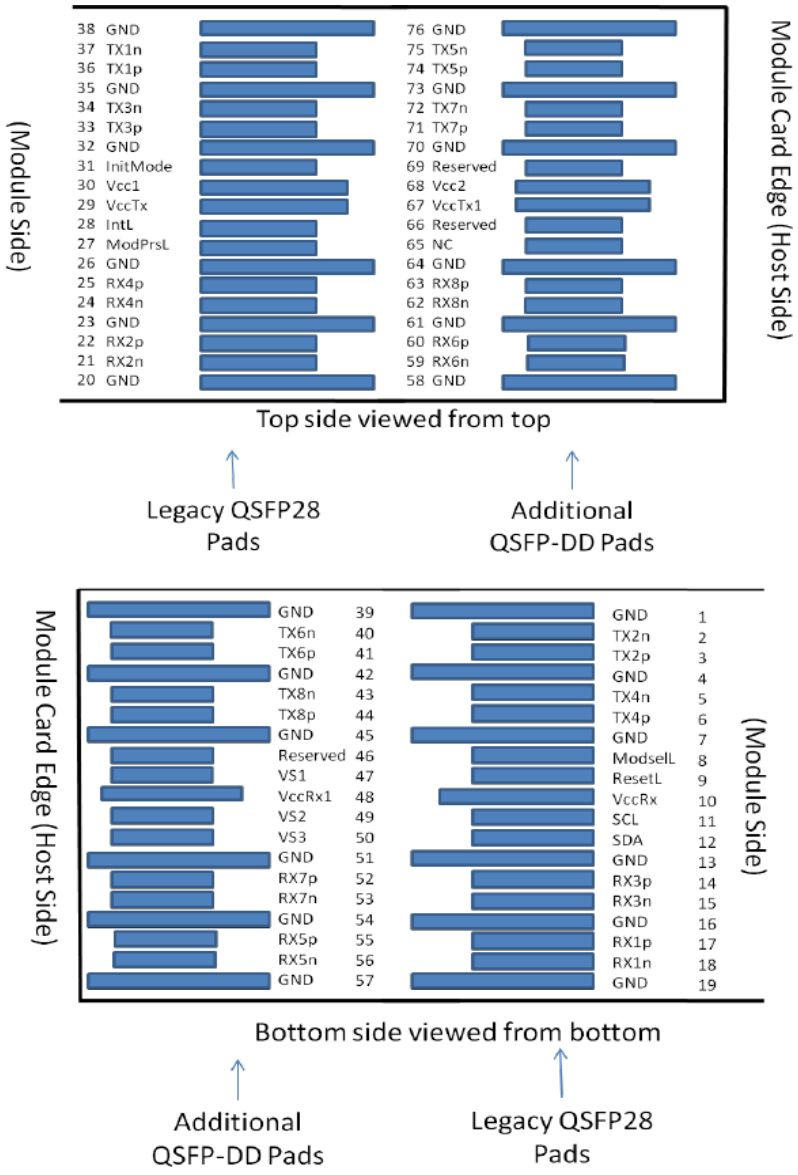
The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	°C	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Pin Assignment

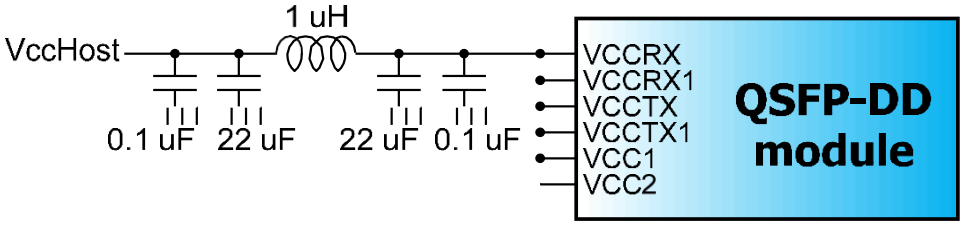


Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	

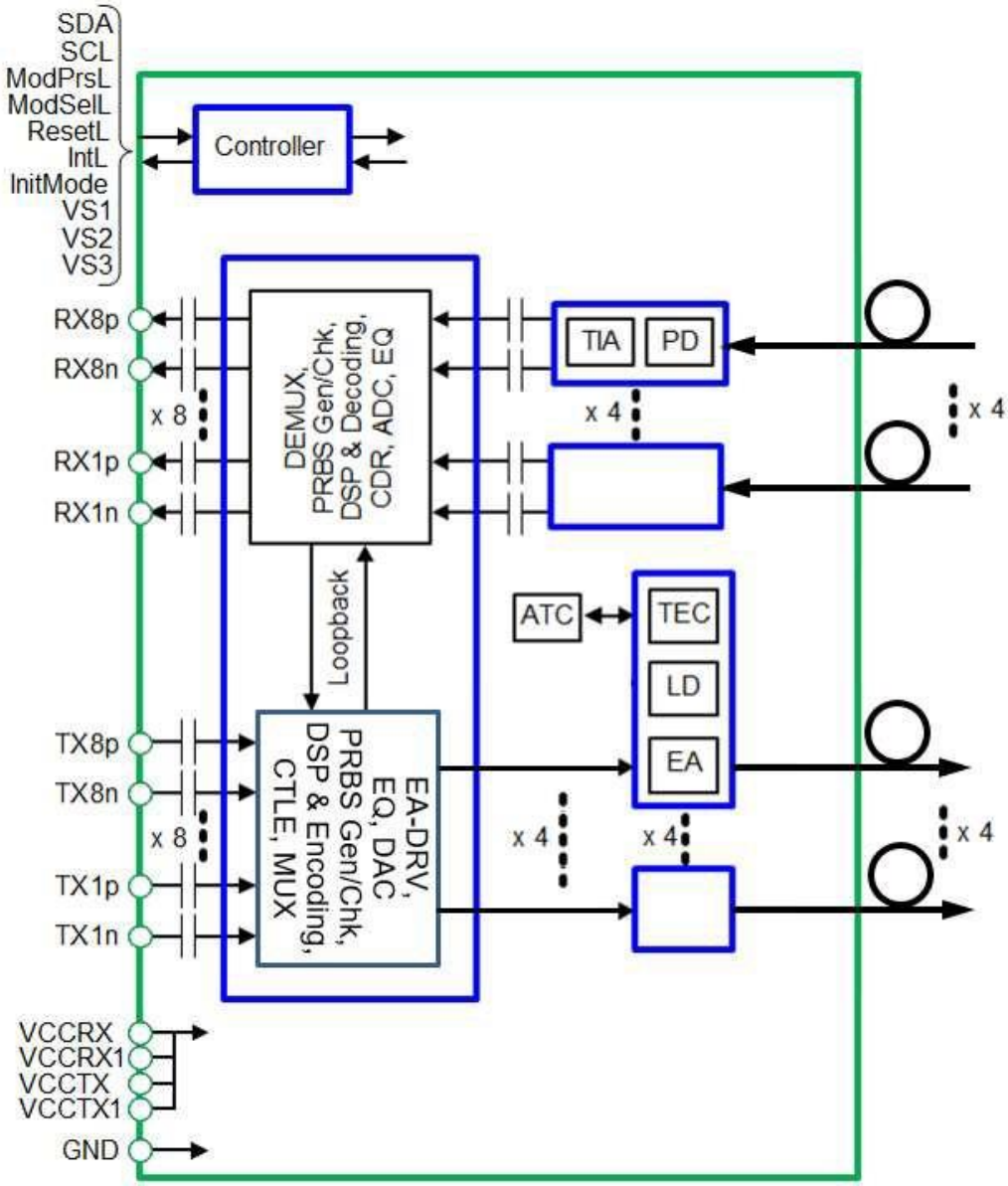
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	1
16		GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	

44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

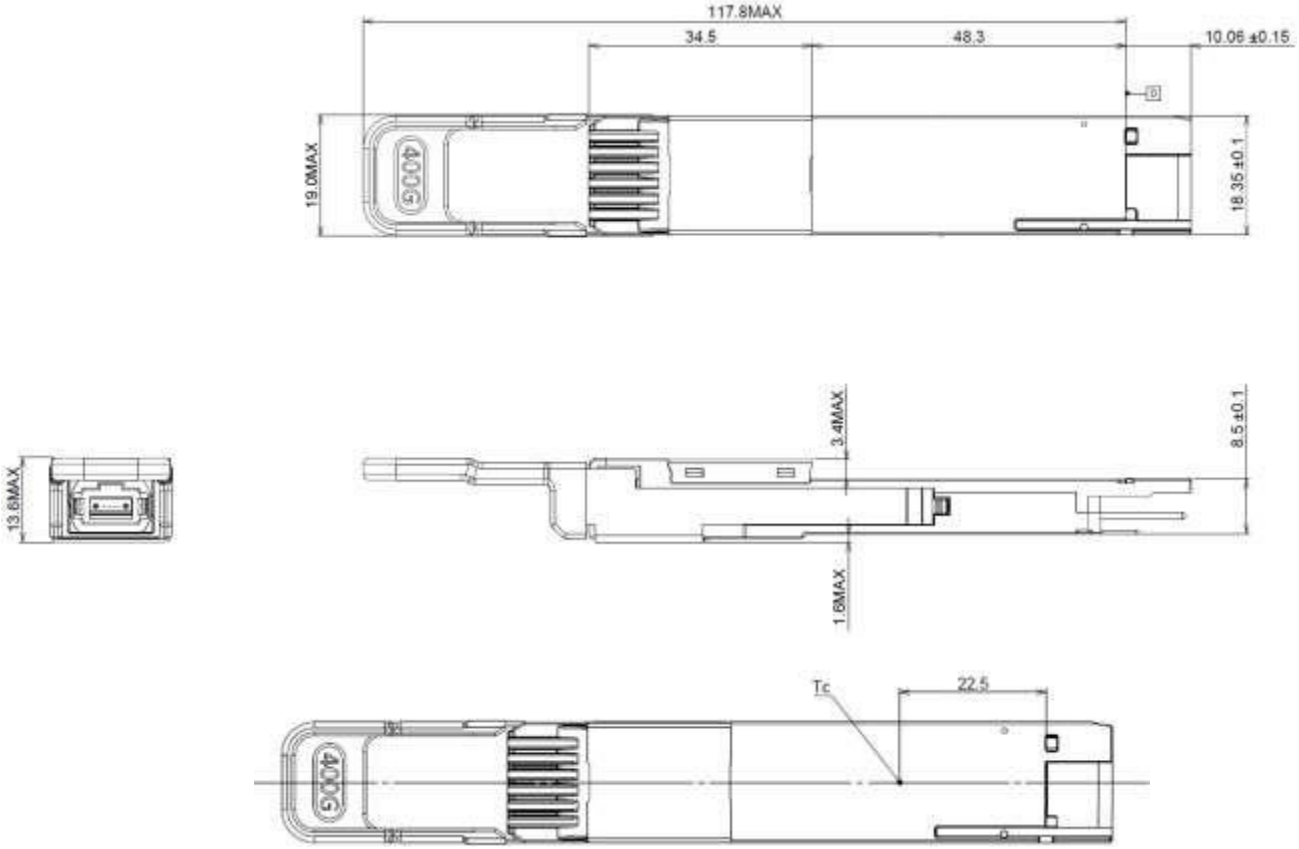
Recommended Power Supply Filter



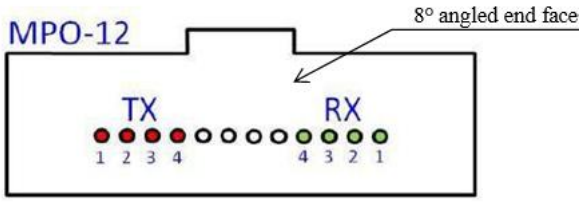
Recommended Host - Transceiver Interface Block Diagram



Mechanical Drawing



Case temperature measurement point



Looking into the connector, transmitter is on the left

Unit: mm

Ordering Information

Part No	Specification									
	Package	Data rate	Laser	Optical Power	Detector	Max. Receive Sensitivity (OMA)	Temp	Reach	Other	Application code
WST-QD4-DR4+C	QSFPDD	4x106.25 Gbit/s	1310nm EML	-3.1~ +4.0 dBm each Channel	PIN	-4.5 dBm each Channel	0~70°C	2km	DDM RoHS	400G Ethernet

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	30-Jun-2021	New Issue	ShaoYu Lee	Tom Tang	Wayne Liao
V1.1	14-Oct-2022	Update Pin Assignment	ShaoYu Lee	Tom Tang	Wayne Liao
V1.2	08-Jun-2023	Update Format	ShaoYu Lee	Tom Tang	Wayne Liao

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